Chapter 4

UC3842

In this chapter we will explore the functions of the control IC, the UC3842. This is a very versatile IC and contains a functionality to build a basic current mode control switched mode power supply.

The functional block diagram of the IC is shown in figure 4.1

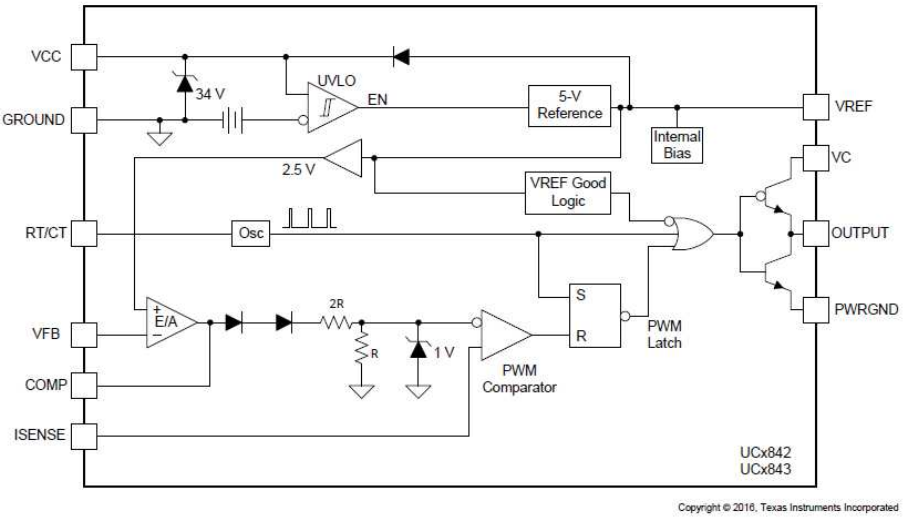


Figure 4.1: Functional block diagram of the UC3842

The pin layout of the IC is shown in figure 4.2. The pin layout is the same for both the PDIP and SOIC packages.

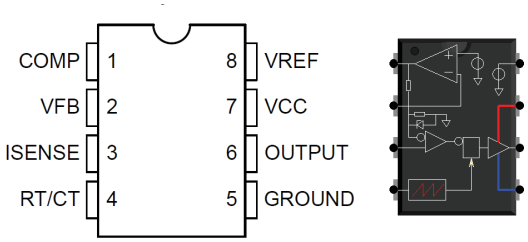


Figure 4.2: SOIC and PDIP package pin layout and Caspoc symbol

4.1 Supply voltage

The supply voltage depends on the type of IC. In table 4.1, the minimum voltages are given, when the IC is turned on and the minimum voltage level that should be maintained, to keep the device on. Also the maximum duty cycle depends on the type. The $UC3844$ and $UC3845$ have maximum duty cycle, which is limited to a maximum of 50%. These types can be used for halve bridge controllers or for limiting the maximum on time in a Flyback converter.

Type	UVLO On	UVLO Off	Max dutycycle
UC3842A	$16.0V$	$10.0V$	$< 100\%$
UC3843A	$8.5V$	$7.9V$	$< 100\%$
UC3844A	$16.0V$	$10.0V$	$< 50\%$
UC3845A	$8.5V$	$7.9V$	$< 50\%$

Table 4.1: Under Voltage Lock Out [UVLO] and maximum duty cycle.

4.2 Reference voltage

The UC3842 comes with an internal reference voltage to feed the oscillator charging. The first test is to measure if pin[8] V_{ref} gives 5 volt. The reference voltage is used to charge the timing capacitor C_T via R_T, as we will see in the next section.

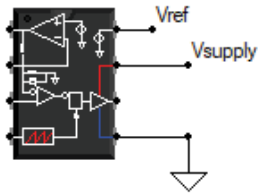


Figure 4.3: Supply voltage and reference voltage V_{ref} .

Our first goal is to see if the UC3842 is active and this is done by measuring the reference voltage on pin[8].

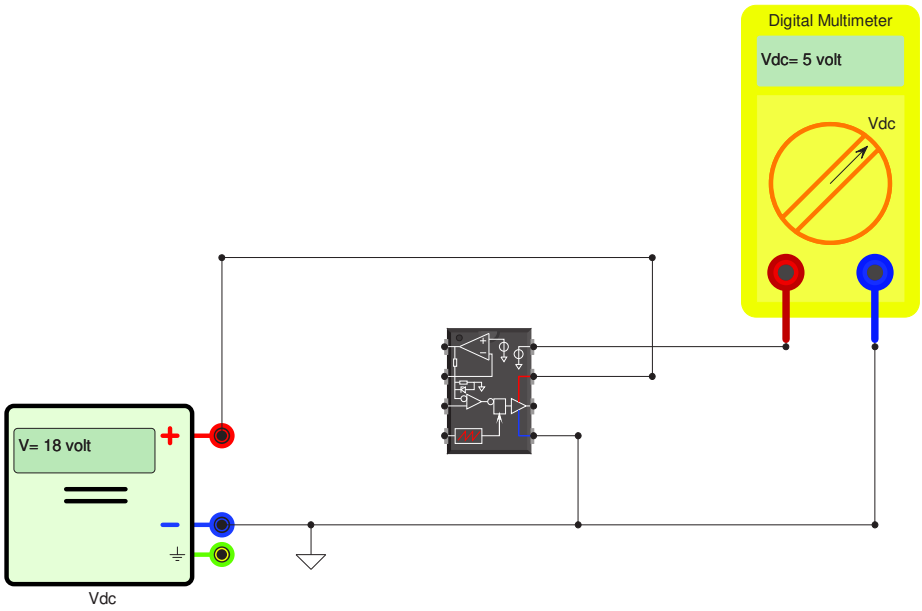


Figure 4.4: Measure V_{ref} on pin[8].

Build the circuit and connect the power supply. Increase the supply voltage from 0 volt to 20 volt, and observe at which supply voltage level, pin[8] V_{ref} gives 5 volt.

Supply voltage V_{supply}	Reference voltage V_{ref}
0	0
5	.
10	.
15	.
16	.
17	.
18	.
19	.
20	.

Table 4.2: V_{ref} as function of V_{supply} for increasing supply voltage.

Decrease the supply voltage from 20 volt to 0 volt, and observe at which supply voltage level, pin[8] V_{ref} gives 5 volt.

Fill in the three boxes in 4.5, to mark the on and off of the UC3842.

Supply voltage V_{supply}	Reference voltage V_{ref}
20	.
19	.
18	.
17	.
16	.
15	.
14	.
13	.
12	.
10	.
5	.
0	.

Table 4.3: V_{ref} as function of V_{supply} for decreasing supply voltage.

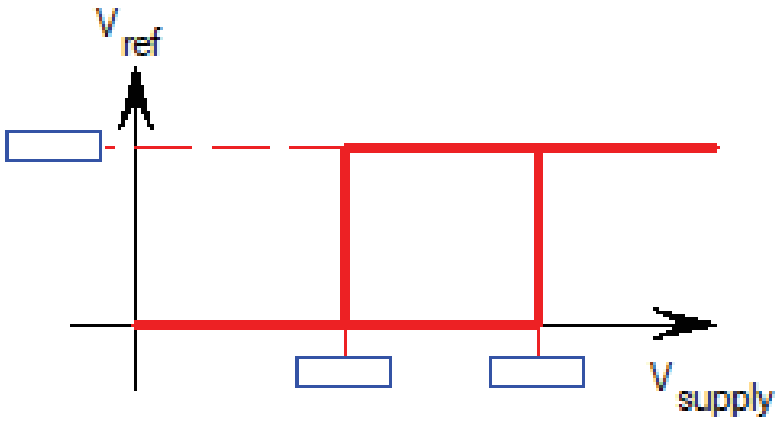


Figure 4.5: Measure the hysterese of V_{ref} depending on the supply voltage V_{supply}.

4.3 Internal oscillator

The switching frequency of the IC is determined by a simple R-C network, which is charged and discharged by the UC3842. It is the heart of the UC3842 and is used not only for controlling the switching frequency, but can also be used as timer for Constant-On Time or Constant-Off Time controllers. Even the signal of the oscillator can be used to create a constant duty cycle control. The basic schematic for hte internal oscillator is given in figure 4.6. The resistor R_T charges the capacitor C_T. If the maximum voltage on capacitor C_T is reached, the capacitor is internally short circuited and its voltage drops to the minimum voltage level, from which the period starts all over gain. As soon as the capacitor voltage start rising, the output pin[7] becomes high.

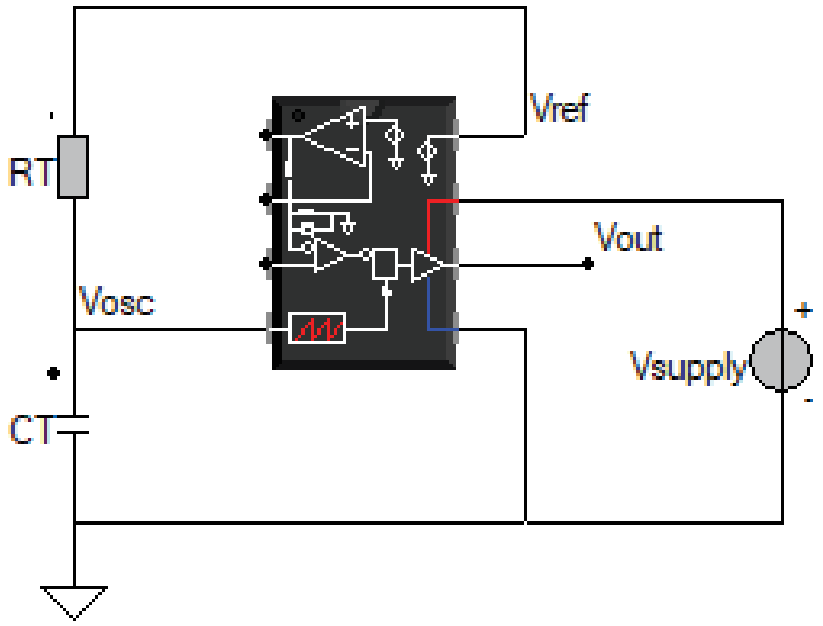


Figure 4.6: Basic circuit for the internal oscillator

4.3.1 Oscillator frequency

The oscillator is based on an external capacitor that is charged by via an external resistor and discharged whenever the maximum capacitor voltage is reached. The charging time of the capacitor is given as

$$T_{charge} = R_T \cdot C_T \tag{4.1}$$

where R_T and C_T are the external resistor and capacitor, as shown in figure 4.7

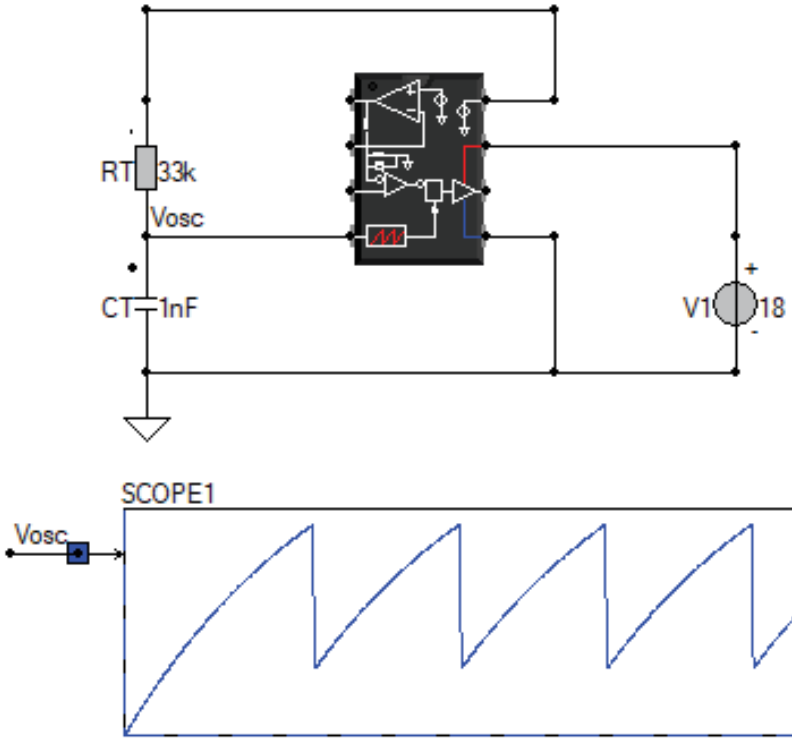


Figure 4.7: External resistor R_T and capacitor C_T define the switching frequency

The capacitor is discharged whenever the maximum voltage reaches approximately $2.7v$. However this varies among different manufacturers.

The oscillator voltage is shown in figure 4.8

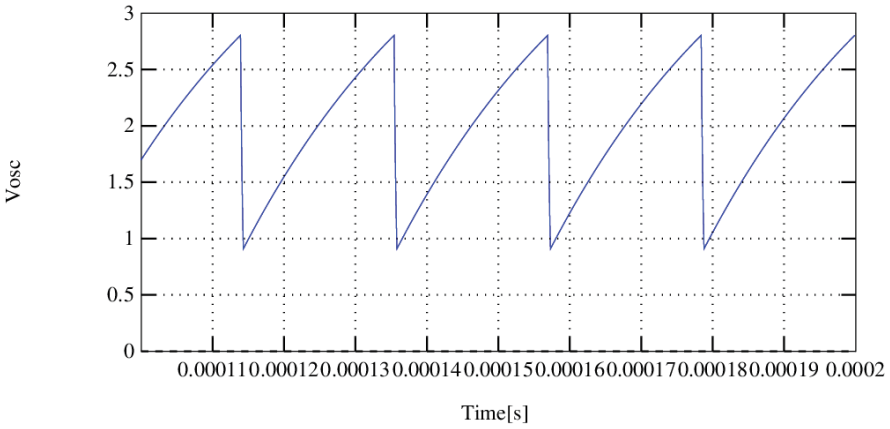


Figure 4.8: Oscillator voltage V_{osc}

Question:

What is the minimum and maximum value of the voltage V_{osc}.

Answer:

Maximum Voltage=[ ]
Minimum Voltage=[ ]

4.3.2 Timing Capacitor and Resistor

The oscillator frequency is given by the timing resistor and capacitor and is related by

$$F_{osc} = \frac{1.72}{R_T \cdot C_T} \tag{4.2}$$

The timing capacitor and resistor can also be read form figure 4.9

4.4 Variable frequency

A variable frequency can be created by adding a variable resistor in series with the timing resistor R_T, see figure 4.10. Use a variable resistance of $100k\Omega$ in series with a fixed resistance of $15k\Omega$, to ensure a minimum frequency defined by the fixed resistor.

The fixed resistor R_T is is used to limit the charging current of the timing capacitor C_T. If you adjust the variable resistor and measure the frequency

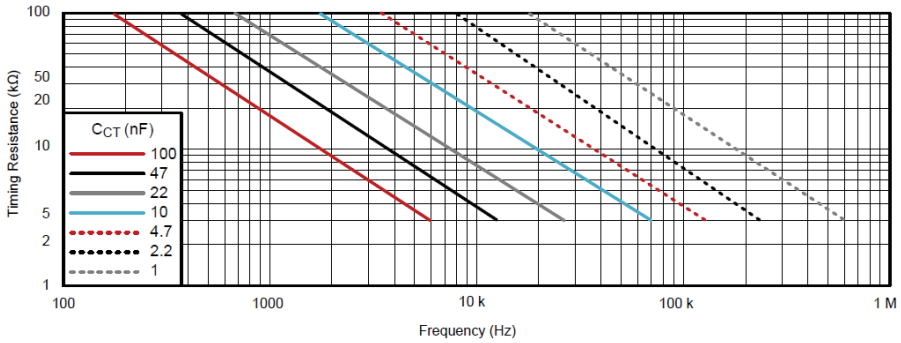


Figure 4.9: Datasheet showing resistor R_T and capacitor C_T for defining the switching frequency

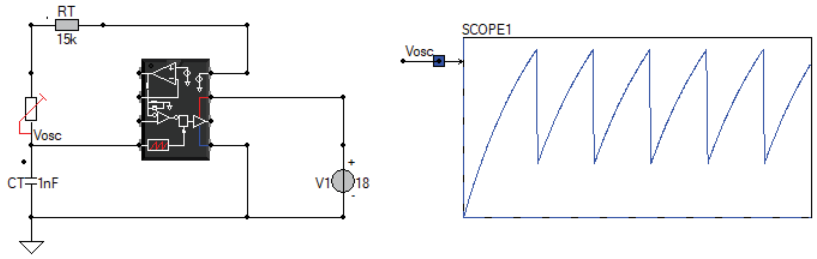


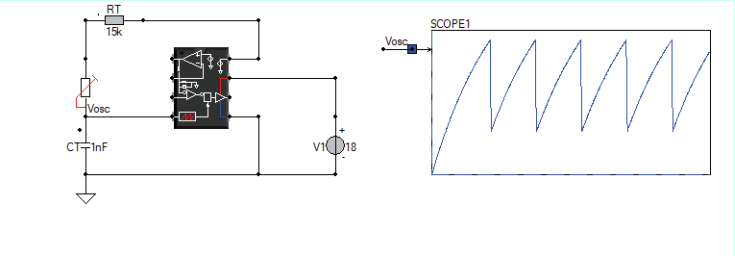
Figure 4.10: Variable oscillator frequency, by adjusting R_T

of the oscillator voltage, the period changes depending on the total resistance, according to figure 4.9.

Question:

Build a circuit to create a adjustable frequency. Adjust the resistance and measure the oscillator frequency. Note the frequency in table 4.4.

Answer:



Variable resistance[Ω]	Oscillator frequency[kHz]
0	.
$5k$	.
$20k$	.
$50k$	.
$75k$	.
$100k$	.

Table 4.4: Frequency of V_{osc} as function of the series resistance.

4.5 Variable dutycycle

Pin [3] $Isense$ is used for implementing peak current mode control. However we can also use it to create a variable duty cycle. As soon as the voltage on this pin crosses the reference value of $V_{ref} = 1$ volt, the output voltage V_{out} is set to zero volt. For a variable dutycycle control, this signal is created from the oscillator voltage $Vosc$.

4.5.1 Isense

The $Isense$ pin is used to turn off the output as soon as the voltage on that pin exceeds 1 volt. Using Isense we can control the duty cycle. If we both measure V_{osc} and V_{out} while pin $Isense$is not connected, we have the maximum dutycycle

Question:

Measure V_{osc} and V_{out}. What is the maximum dutycycle?

Answer:

The maximum dutycycle is given by the value of C_T, as shown in fig. 4.11

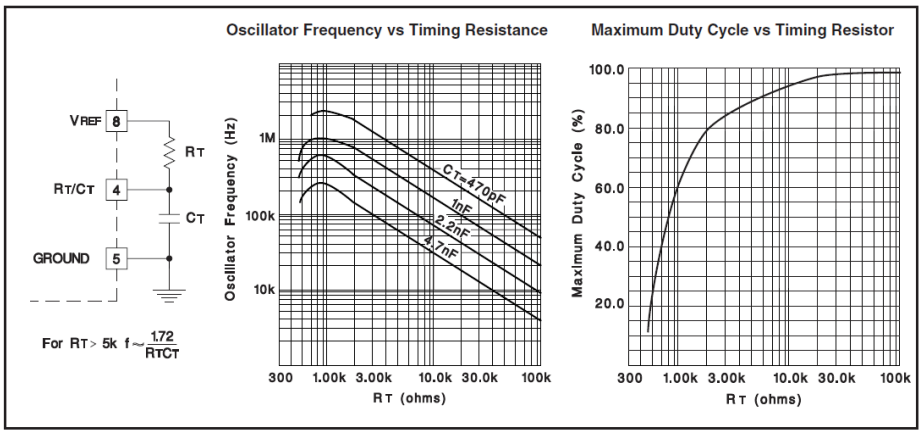


Figure 4.11: Oscillator Section, copyright: Datasheet Unitrode

Choose a low capacitor value C_T, in order to have a larger value for R_T, as this will result in a lower current drawn form the V_{ref} reference voltage pin[8]. Figure 4.12 shows the oscillator voltage and the output voltage.

Since $Isense$ remains below 1 volt, the output V_{out} remains high with the maximum duty cycle, see figure 4.13.

The maximum dutycycle is defined by the size of the timing capacitor C_T as defined in figure 4.14.

If we would have a controllable signal that crosses the reference voltage of $V_{ref} = 1$ volt, during the on-time, we would be able to control the duty cycle. We can create this signal from the oscillator voltage V_{osc}, but this signal should bot be disturbed, in order not to influence the timing of the oscillator. Therefore we need to buffer the oscillator voltage V_{osc}.

Depending on the manufacturer of the UC3842, the minimum and maximum value of V_{osc} vary. The original UC3842 from Unitrode, varies between $!.8 < V_{osc} < 3.5$. In the datasheet, only the voltage amplitude of $\hat{V_{osc}} = 1.7$ volt is defined. Some manufacturers have a lower minimum oscillator voltage, less than 1.7 volt.

To use the oscillator voltage V_{osc} for controlling the dutycycle, we need a transistor to buffer the oscillator voltage. Unitrode recommended the circuit as given in figure 4.15.

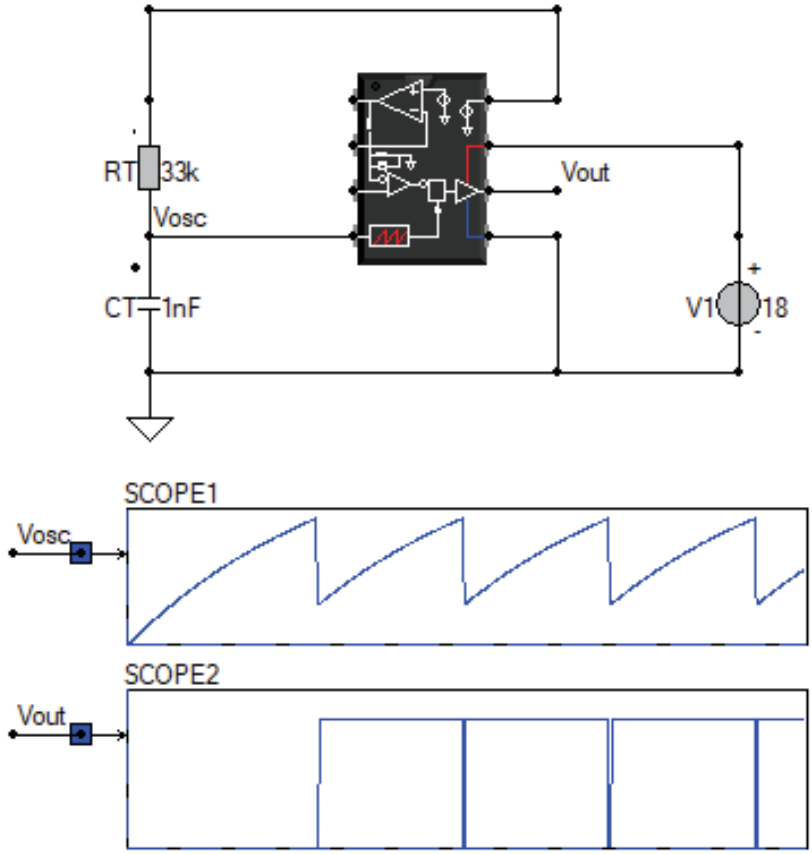


Figure 4.12: Maximum duty cycle

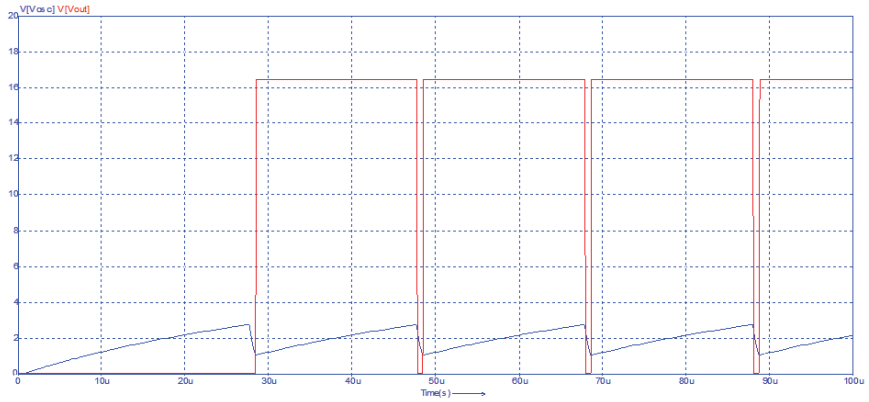


Figure 4.13: Maximum duty cycle

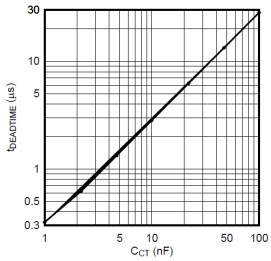


Figure 4.14: Maximum duty cycle given in μs as function of the timing capacitor C_T

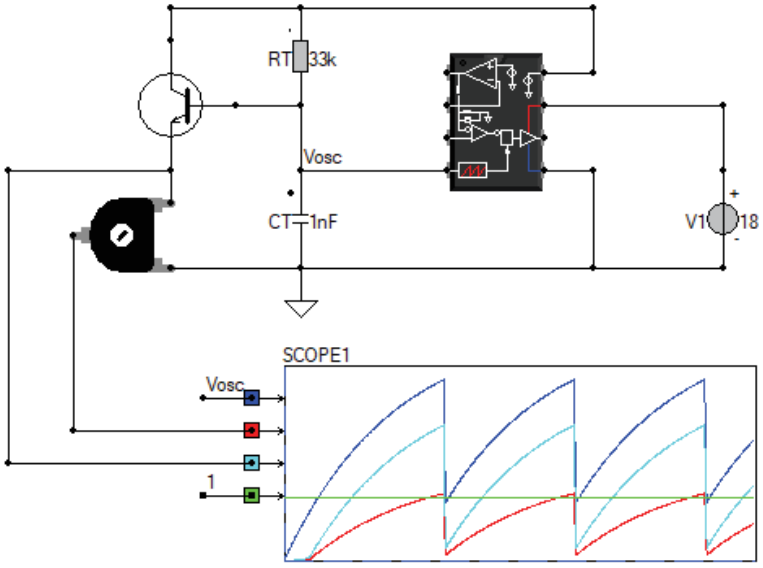


Figure 4.15: Buffering the oscillator voltage to derive a control signal for variable duty cycle.

The voltage at the $Isense$ pin[3] is approximately 0.7 volt less the oscillator voltage $Vosc$. If the minimum voltage of V_{osc} is less than 1.7 volt, the maximum possible voltage at $Isense$ at the beginning of the period is also less than 1 volt, due to the voltage drop $V_{be} = 0.7$ volt of the NPN transistor. Therefore it will not be possible to have a duty cycle of 0%

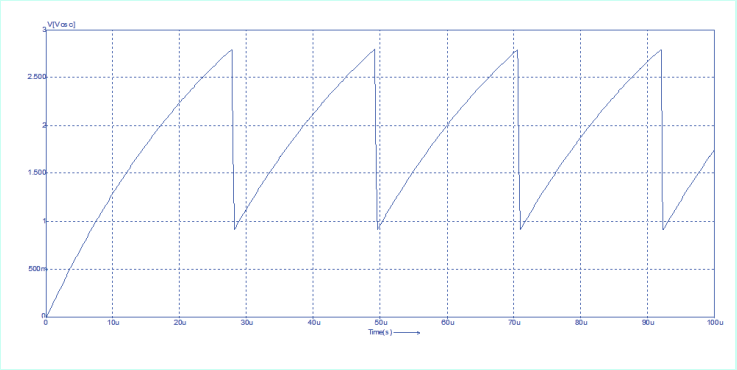
A second PNP transistor is required to shift the level of the oscillator voltage above the reference voltage of 1 volt. Therefore we are using a second PNP transistor to increase the voltage level. A PNP transistor is first buffering the oscillator voltage and because of the $V_{be} = 0.7$ voltage drop, the oscillator voltage is now increased by 0.7 volt, see figure 4.16.

Question:

Measure V_{osc} and write down the maximum and minimum voltage.

Answer:

$V_{osc}^{max} = [\quad\quad\quad\quad]$
$V_{osc}^{min} = [\quad\quad\quad\quad]$



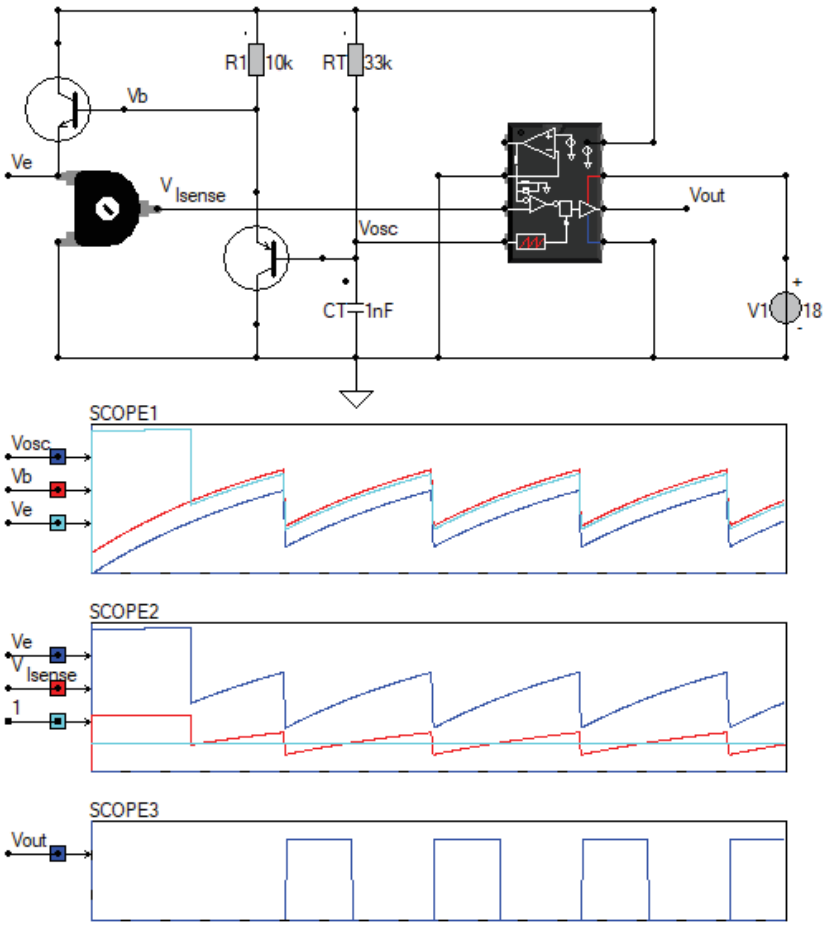


Figure 4.16: A PNP transistor is used for buffering V_{osc} and increasing the voltage level by 0.7 volt.